4200 series
Advanced Manufacturing Test System

A range of advanced manufacturing test systems offering a wide range of test methods and high throughput capability

4200 - ADVANCED MANUFACTURING TEST SYSTEM

- Maximum of 2048 pins
- Windows 95 or NT operating system
- Automatic program generation software
- Graphical program debug capability
- Autodebug facility
- Inductive and capacitive vectorless test
- ISP and FLASH programming

Introduction

The 4200 series is the flagship of the IFR range of automatic test equipment. Designed to be the fastest manufacturing test system on the market, it is ideally suited to high volume manufacturing operations where throughput is of paramount importance. With an established customer base, the system tests a wide variety of printed circuit boards covering applications such as telecoms, automotive and consumer electronics, amongst others.

By achieving the highest level of fault coverage, and testing product in the shortest possible time, the 4200 series reduces capital investment by providing a single test station within the beat rate of the production line. Quite simply, a single 4200 series tester can perform a task which would require several competitive systems.

Architecture

The 4200 series is controlled by an industry standard PC with a choice of Windows 95™ or NT™ operating systems. The graphical user interface has been designed to provide a familiar environment allowing new users to quickly progress along the learning curve.

Within the range, there are currently two systems, the 4215 and 4220. The differences lay in the testpoint and power supply capacity:

4215 - Maximum of 1152 universal testpoints & three user power supplies

4220 - Maximum of 2048 universal testpoints & six user power supplies

Both systems use a cardcage architecture and can be fitted with a range of cards selected from the following list to provide the most appropriate configuration:

Analog In-Circuit card
Universal In-Circuit card
General Purpose Input/Output card
Instrument Access card

Analog and Digital Testing

The key to low test times is the optimization of analog tests, including contact, shorts and opens. The 4200 series offers a combination of high speed and exceptional accuracy through innovative pipeline and parallel processing techniques. A further factor is the utilization of advanced DSP measurements.

High guarding ratios and multiwire measurements ensure component isolation and accurate diagnostics during In-Circuit tests. The ability to change all parameters associated with a measurement is vital to achieving the highest possible accuracy.

For mixed signal testing, such as ADC, DAC and CODEC devices, the 4200 series fully integrates its analog and digital capability. Every pin is backed by analog and digital resources, and their ability to be used in conjunction with each other is a vital element in testing this important category of devices.

Every pin is provided with terminators to enable the testing of tristate buses and open collector devices. Slew-rate controlled pin drivers ensure that vectors delivered to the testpoint are high integrity and load tolerant. Where necessary, full backdriving protection is provided.

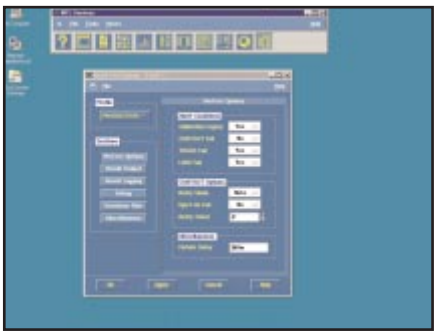
For the testing of free running devices, 50 MHz clock synchronization and phase locking is provided. Vector rates of 5 MHz with 20 ns edge placement ensure that dynamic devices maintain keep-alive speed. Testing the most complex VLSI devices requires a range of advanced features such as hardware triggers, pin formatting and variable timing sets. On-the-fly jumps allow for program flow decisions to be made not only within the test program but also within individual digital tests.

The effectiveness of the 4200 series is further enhanced by the ability to program FLASH devices and utilise the capability of Xilinx™ or Lattice™ ISP chips. In the case of FLASH programming, this negates the need to invest in further equipment, adding extra value to the In-Circuit stage of the process.

4200 series

Test Language

The test language provided with the 4200 series provides the user with a high level structured programming environment with fully integrated edit and debug facilities. The structure offers the twin benefits of top level simplicity whilst also allowing the control of all system parameters at a lower level.



Test Executive

Simple language statements specify 'packaged' tests for common types of measurement, selecting appropriate stimuli settings and measurement ranges automatically, reflecting the circuit configuration. These default settings can be altered by adding modifiers to the standard command.

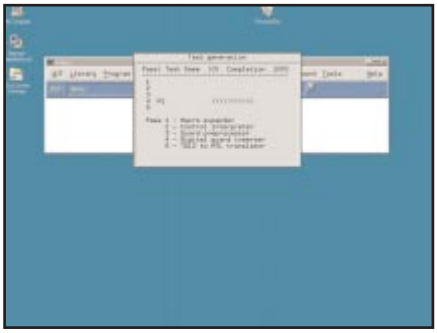
Although a compiled language, full interactive edit and debug is achieved through a high speed incremental compilation process. The overall effect is the speed and power of a compiled language combined with the interactive nature of an interpreted language.

The graphical user interface features a menu system providing control of input/output and peripherals such as barcode readers and printers. Numeric data can be expressed in decimal, hexadecimal, octal and binary. Electrical engineering notation (e.g. 10 mV) is also fully supported for applications orientated manipulation of test parameters and results.

Test Program Generation

Test programs are normally generated from the CAD data used to describe the board under test. The IFR FABmaster package is used to link to a wide range of CAD formats, producing a .CB format circuit description file and enabling fixture customization. The .CB file is then used to create a program using the IFR CAPG (Computer Assisted Program Generation) package.

This approach ensures that time-to-market is maintained by quick and accurate creation of fixture and program data. In order to reduce the subsequent debug time, CAPG uses a simulator to apply the necessary guards to the test program.



Computer Assisted Program Generation

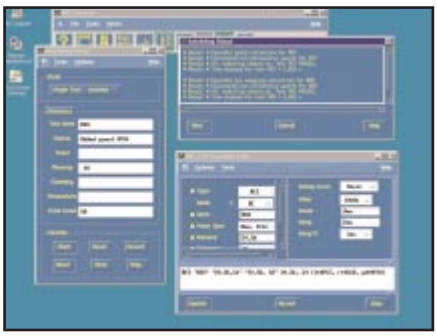
All of the test methods supported by the 4200 series are fully integrated into CAPG. The interface is designed to allow the test engineer the maximum flexibility in using the most appropriate test for each device present on the board.

Graphical Debug Tools

A suite of debug tools is used to quickly commission the test program and fixture, again reducing the time-to-market aspects to the test process. In the case of analog measurements, a histogram display is used to dynamically display results with reference to nominal values and tolerances. Digital tests show state and timing information across the whole of the pinface in use during a particular test. Flow trace and test structure diagrams are also provided, fully integrated into the test editors. Each tool within the graphical debug suite gives point and click access to the whole range of parameters applicable to the test.

Autodebug

This facility is designed to improve time-to-market by using automatic debug algorithms, independent of the programmer. By altering the range of measurement parameters and analyzing the subsequent results across a number of reiteration modes, the autodebug facility is able to quickly commission a high proportion of analog In-Circuit tests. The graphical user interface allows user selection of all parameters to ensure the best results in the time available. Essentially, the autodebug facility mimics the actions of a human programmer without the programmer being present, for instance overnight.



Autodebug

Boundary Scan

The 4200 series fully supports the IEEE 1149.1 boundary scan standard for overcoming access and testability limitations. Automatic test generation is provided for boundary scan devices appearing singly or within scan paths. These tests are derived from the CAD data describing the board and the BSDL (Boundary Scan Description Language) file pertaining to each device. The process is automatic and fully integrated into the IFR CAPG facility.

Functional Cluster Testing

The cluster test facility is used to define and test the functionality of a number of components as a single logical entity. For instance, the individual components of an amplifier circuit could be tested individually using the In-Circuit capability, followed by a test to ensure that the full amplifier circuit is performing correctly.

Usually, the requirement to perform a cluster test is stimulated by one of two circumstances. Firstly, cluster testing is a useful method of overcoming test access, allowing test to be performed from the access points provided. Alternatively, the throughput capability of the 4200 series often leaves extra time within the beat rate that can be utilized by performing the functional tests that would otherwise necessitate further test system investment.

Third-Party and System 80 Compatability

By selection of the appropriate fixture adapters and program conversion software, the 4200 series can effectively test using applications initially written for third-party competitive test systems.

A specific example of this capability is the ability to use System 80 programs and fixtures. The translation software has been written to preserve the parameters and guards associated with each test in the older program, minimizing the time taken to move to the new platform.

Fixturing

In order to offer the maximum flexibility and reliability, the 4200 series uses the full range of IFR vacuum and pneumatic fixtures. Where necessary, more esoteric applications can be accommadated using the customized fixture capability of IFR's Production Test Services facility.

In addition to IFR's fixturing capability, a wide range of third party suppliers also offer fixtures for the 4200 series.

Vectorless Testing

IFR Limited is unique in offering both inductive and capacitive vectorless techniques, ensuring wide test coverage across a range of components from complex ASICs to connectors. Inductive probing is performed using the IFR patented Q-test II technique, whilst capacitive tests use the industry standard HP TestJet™ probe. The presence of two alternatives for vectorless testing allows the test engineer to use the most appropriate for a given application, essentially matching the pros and cons of

each technique to the devices under test. These two techniques contribute to the system's ability to generate tests for devices quickly, and to accurately diagnose faults to enhance productivity and quality.

Production Line Integration

The 4200 series is designed to easily integrate into a high volume production line or to be used manually by an operator.

By selecting the horizontal interface, in conjunction with the correct height setting, the 4200 series conforms to both SMEMA and de-facto European standards for manufacturing automation. A number of in-line handlers, from a variety of suppliers, have been integrated with the system, supported by the necessary communication protocols.

Specification

General Test Capabilities
Full in-circuit test (analog/digital/mixed signal)
Boundary-Scan test
Bus emulation
Partitioned functional test
Q-Test
Analog functional

Computer System (minimum)
Pentium PC (200 MHz)
17 in, 44 cm SVGA 1024 x 768 monitor
PCI Bus
32 MBytes RAM
Windows NT/95
IEEE-488 interface (option)
Serial ports
Tape streamer option
Bar Code Reader option

Testpoint Count
4215 128-1152 analog or universal testpoints
4220 128-2048 analog or universal testpoints
Multiplexing ratio 4:1
128 testpoints per card

Analog Test Facilities

Contact test	<100 kΩ
Shorts test	1-100 Ω
Link test	1-100 Ω
Resistance DC	0 Ω-10 MΩ
Resistance AC	0 Ω-1 MΩ
Capacitance AC	0 pF-100 mF
Capacitance DC	1 µF-100 mF
Inductance	0 H-100 H
Diode	ON OFF
Zener	Voltage
FET	ON OFF RDS
LED	ON OFF
Transformer	Ratio 0.001-100
Opto-isolator	
Transistor	ON OFF HFE

General Purpose Analog Facilities

DC stimulus (2 off)	1 mV-25 V 0 A-100 mA
AC voltage stimulus	0.1 V-20 V pk-pk
Frequency	0.1 Hz-20 kHz
Noise	<10 mV pk-pk 20 MHz b/w
Waveshapes	sine, square, triangle, ramp up/down
DC voltage measurement	0 V-±50 V
DC current measurement	0 A-±100 mA
AC voltage measurement	0 V-50 V
Frequency measurement	0.02 Hz-5 MHz
Period measurement	10 µs-65 s
Programmable resistor	0 Ω, 1 Ω-10 MΩ in decade steps voltage limiter

1149.1 Boundary-Scan Facilities (Option)
Any standard testpin may be used to perform Boundary-Scan tests. A configurable memory is accessible to all testpins providing the serial data needs for Boundary-Scan testing and permitting support for multiple scan paths.

Serial data memory	128 kbit (reloadable)
Input/Output levels	Uses standard digital drives (see below)
Tests supports	Integrity tests Interconnection tests Virtual in-circuit tests Cluster tests Device self tests

Digital Testing
Digital testing is full parallel drive, parallel sense.

Pattern rate	5 MHz – multiple transitions per test step
Internal clock frequency	50 MHz
Clock divider	1-256
Test step period	200 ns min with phase set movements
Phase step period	20 ns
Timesets	4
Formats per time set	6
External clock phase lock	50 MHz
Hardware Event Triggers	4
Phase lock multiplier	1-16
External sync up to 50 MHz	
Pattern generators (shift, rotate, increment) accessible to all pins	
Flow control Instructions	NOP, IF(NOT), CALL, RETURN, JUMP DELAY, LOOP, EXITLOOP, ENDLOOP, REPEAT, UNTIL, STOP, PAUSE
Max Input Volt	–50 V-+50 V (logic relay open)
Control RAM depth	8 K
Flow trace RAM	64 K
Signature analysis	per pin
Logic Families	1 per board
Drive high voltage range	–1.0 V-+14 V
Drive low voltage range	–6.0 V-+1.0 V
Sense levels	–8.0 V-+15 V
Drive high/low current	500 mA (forcing) 50 mA (non-forcing)
Slew rate	50 V/µs (slow) 150 V/µs (fast)
Output impedance	2 Ω (forcing) 10 Ω (nonforcing) nominal
Backdrive timeout	10 µs-650 ms
Relaxation timer	1 ms-10 s
Testpin RAM depth	8 K
Pin face skew	20 ns
Digital Guarding	2 static guards per TP board one high one low

Debug Facilities
Manual probe for in-circuit debug and reverse trace functional test diagnostics
Pin scan and search
Bugprobe

Busfail

UUT Power Supplies
4215 Maximum 3 supplies
4220 Maximum 6 supplies

2 types available:
0.15V-6.0V, 25A voltage and current programmable
1.0V-30.0V, 7A voltage and current programmable

System Software

MTL Test Language
High level, function based, structured programming language
Interactive edit and debug facilities
System self check
System self calibration

CAPG (Computer Assisted Program Generator) Option
PC WIN 95/NT
Generic device library
CAD or manual input
Safe check digital backdriving analysis software
Extensions for bus emulation
Boundary-Scan test generation
Reverse trace for partitioned functional testing

FABmaster CAD interface (Option)

***i*-Base Information Management System (Option)**

Operating Conditions

Mains supply	180-265 volts, 47 Hz-63 Hz, single phase 13 A
Power consumption	2 kVA
Operating temp range	+10°C-+35°C
Humidity range	25% RH-75%RH

Dimensions

Height	Depth	Width
1.255 m	1.095 m	1.5 m

Weight
227 kg

Vacuum Actuation
–20 in Hg (–0.66 Bar) to –28 in Hg (–0.94 Bar)

System Compatibility
System80/M530 fixture adaptor for cannon style fixture.
INCITE test program conversion software

Fixturing
Vacuum operated interface

System interface life	>30,000 operations
Fixture to interface life	>5,000 operations

IFR Americas, Inc., 10200 West York Street, Wichita, Kansas
67215-8999, USA. E-mail: info@ifrsys.com
Tel: +1 316 522 4981 Toll Free USA: 1 800 835 2352 Fax: +1 316 522 1360

IFR Ltd, Longacres House, Norton Green Road, Stevenage, Herts
SG1 2BA, United Kingdom. E-mail: info@ifrinternational.co.uk
Tel: +44 (0) 1438 742200 Freephone UK: 0800 282 388 Fax: +44 (0) 1438 727601

Part no. 46891-069
Revision A